AMENDMENTS TO THE CLAIMS:

Please amend claims 6-12 as follows:

6. (Amended) A method [of manufacturing integrated circuit chips,] for testing semiconductor integrated circuits, the method comprising:

providing a semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged [theron] thereon in two columns and at least two rows, each of said plurality of semiconductor integrated chips having a plurality of external terminals;

coupling a probe card to the semiconductor wafer through a plurality of probe needles on said probe card corresponding to said plurality of external terminals of each of said integrated circuit chips, said probe card receiving a plurality of independent test signals and a power supply signal from a tester, wherein said probe card includes structure defining a rectangular through hole having first and second long sides, and wherein the probe needles extend through the rectangular through hole;

concurrently supplying the independent test signals and the power supply signal from the tester through the probe needles to said plurality of external terminals of said plurality of integrated circuits; and

concurrently measuring electric characteristics of said semiconductor integrated circuit chips in an independent manner.

7. (Amended) The method [of manufacturing] of claim 6, wherein said external terminals are centrally disposed within said integrated circuit chips, with integrated circuits on either side of said external terminals.

8. (Amended) The method [of manufacturing] of claim 7, wherein said external terminals are arranged in a plurality of columns and rows.

9. (Amended) The method [of manufacturing] of claim 8, wherein the step of providing a semiconductor wafer [said providing] includes forming memory arrays for each of said integrated circuit chips.

10. (Amended) The method of [manufacturing according to] claim 6, wherein the test signal and the power supply signal are supplied from said tester to said probe needles by way of a plurality of wiring lines on internal layers of said probe card.

11. (Amended) The method of [manufacturing according to] claim 6, wherein the test signal and the power supply signal are supplied from said tester to said probe needles by way of a plurality of wiring lines on different internal layers of said probe card, said wiring lines positioned on different ones of said different internal layers according to a type of signal carried by said wiring lines.

12. (Amended) A probing test method of semiconductor integrated circuits, comprising:

preparing at least one semiconductor wafer, said semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged thereon in rows and columns, said semiconductor integrated circuit chips having a plurality of external pads;

preparing at least one probe card, said probe card having a plurality of connection terminals for receiving from a tester a test signal and a power supply signal, said at least one probe card having a plurality of probe needles corresponding to said plurality of external pads, respectively, wherein said probe card includes structure defining a rectangular through hole having first and second

long sides, and wherein the probe needles extend through the rectangular through hole;

supplying said test signal and said power supply signal from said tester to said probe needles by way of said connection terminals in a completely independent manner;

supplying said test signal and said power supply signal from said probe needles to said semiconductor integrated circuit chips, by way of said external pads, in a completely independent and concurrent manner; and

measuring electric characteristics of the semiconductor integrated circuit chips in a completely independent and concurrent manner.

Claim Status

The original patent included five claims.

Claims 6-16 were added in the reissue application.

Claims 6-12 are amended in this paper.

Claims 1-16 remain pending for examination.

Support for Claim Amendments

In claim 6: [of manufacturing integrated circuit chips,] for testing semiconductor integrated circuits, the method . . . .

Support for this amendment appears at column 4, line 58 – col. 5, line 7 of U.S. Patent No. 5,818,249.

In claim 6: [theron] thereon.

This merely corrects a minor error of spelling and does not change the substance of the claim.

In claim 6: wherein said probe card includes structure defining a rectangular through hole having first and second long sides, and wherein the probe needles extend through the rectangular through hole.

Support for this amendment appears in Figure 3 and at col. 4, lines 39-52 of the '249 patent.

In claims 7-9: [of manufacturing].

These amendments merely conform the preambles of these claims to that of claim 6.

In claims 10 and 11: [manufacturing according to].

These amendments conform the preambles of these claims to that of claim 6.

In claim 12: wherein said probe card includes structure defining a rectangular through hole having first and second long sides, and wherein the probe needles extend through the rectangular through hole.

Support for this amendment appears in Figure 3 and at col. 4, lines 39-52 of the '249 patent.